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An Efficient Method for Multi-bit Correction using BCH

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Abstract:

Transmission of information through a physical medium or wireless medium ,possibility that data get corrupted this leads to an error in a random only selected locations of a symbol or the entire symbol. To have a reliable communication through a communication channel that has an acceptable Bit Error Rate(BER) error correcting codes are used .These codes are used to detect and correct a specific number of error which may occur during transmission of message over a communication channel. As the complexity of communications and signal processing systems increases, so does the number of blocks or elements that they have. The increase in complexity also poses reliability challenges and creates the need for fault-tolerant implementations. In those complex systems, it is common that some of the filters operate in parallel to provide the error free output to the filters by using hamming code in redundant module. It is used for single fault corrections papers. In this paper few methods are proposed for the multiple bit error corrections. The BCH code is used for the multiple error corrections. The encoding ,decoding ,syndrome and error corrections are also discussed. This method shows more reliability with the single error correction implementations existed upto now. BCH codes are widely used in the area like ,mobile communication, Digital communication, Satellite communication ,Optical and Magnetic storage system and Computer
Network etc.

Index Terms- parallel filters, Coding, Error correction codes (ECCs), BCH

I INTRODUCTION

SINGLE ERROR CORRECTION

Parallel filters are commonly found in modern signal processing and communication systems [1]. In many cases, the filters perform the same processing on different incoming signals as there is redundancy to use multiple-input–multiple-output systems [2].This parallel operation can be exploited for fault tolerance. In fact, reliability is a major challenge for electronic systems[3]. In particular, soft errors are an important issue, and many techniques have been proposed over the years to mitigate them[4]. Some of these techniques modify the low-level design and implementation of the integrated circuits to prevent soft errors from occurring. Other techniques work at a higher abstraction level by adding redundancy that can detect and correct errors. One classical example is the use of triple modular redundancy (TMR) in which the design is tripled and a majority vote of the outputs are used to correct errors. Another example is the use of error correction codes (ECCs) to protect the bits stored in memory devices [5]. In this case, a number of parity checks are computed and stored in the memory so that errors can be detected and corrected when the data are read. Finally, for applications that have regular structure and properties, those can be exploited to detect and correct errors with a lower cost than TMR. This is the case for many signal processing circuits [6]. In many cases, ECCs or specific protection techniques are

combined with TMR to achieve a complete protection. For example, the ECC encoders and decoders may be protected with TMR to ensure that they are not affected by errors. In those cases, TMR is used to protect a small part of the circuit that cannot be protected by the ECC or the specific technique. The protection of digital filters has been widely studied. For example, fault-tolerant implementations based on the use of residue number systems or arithmetic codes have been proposed [7], [8]. The use of reduced precision replication or word-level protection has been also studied [9], [10]. Another option to perform error correction is to use two different filter implementations in parallel [11]. All those techniques focus on the protection of a single filter.

II PROPOSED WORK

MULTIPLE ERROR CORRECTION CODES

Bose Chaudhuri Hocquenghem (BCH):

It is discovered by Hocquenghem in 1959 and independently by Bose and Chaudhuri in 1960. It is the powerful random error-correcting cyclic code which is used to correct multiple errors[13]. It makes block size(n) smallest for given message block(k) to obtain desired hamming distance. Its Most important subclass are Reed-Solomon (RS) codes. Berlekamp's iterative algorithm and Chien's search algorithm are most efficient decoding algorithms.In technical terms a BCH code is a multilevel cyclic variable-length digital error-correcting code used to correct multiple random error patterns.

- For positive pair of integers $m \geq 3$ and t, a (n, k) BCH code has parameters:
- Block length: $n = 2^m - 1$

Number of check bits: $n - k \leq mt$

Minimum distance: $d_{\min} \geq 2t + 1$

- $t<(2^m - 1)/2$ random errors detected and corrected.
- So also called 't-error correcting BCH code'.
- Major advantage is flexibility for block length and code rate.
- Generator polynomial → specified in terms of its roots from Galois Field GF(2^k).
- g(x) has $\alpha, \alpha^2, \ldots, \alpha^{2t}$ and their conjugates as its roots.
- We choose g(x) from $x^n + 1$ polynomial factors by taking x^{n-k} as highest term.
- Then the generator polynomial is: g(x)=LCM{ϕ(b+1),ϕ(b+2),…….,ϕ(b+2t) }

The parameters of some useful BCH codes are:

n	k	t	Generator Polynomial
7	4	1	1 011
15	11	1	10 011
15	7	2	111 010 001
15	5	3	10 100 110 111
31	26	1	100 101
31	21	2	11 101 101 001
31	16	3	1 000 111 110 101 111
31	11	5	101 100 010 011 011 010 101
31	6	7	11 001 011 011 110 101 000 100 111

In this paper, (15, 7) BCH encoder and decoder is implemented on Spartan 3E FPGA. For designing the BCH codes, two coding techniques are used .They are systematic codes and Non systematic codes. In case of systematic codes original message d(x) is as it is in the encoded word c(x). where as in case of non – systematic code encoded word c(x) is obtained by multiplying message d(x) with generator polynomial G(x).Hence message data will not be same in the encoded code word

BCH ENCODER:

A (15, 7) BCH Encoder is as shown in fig-1

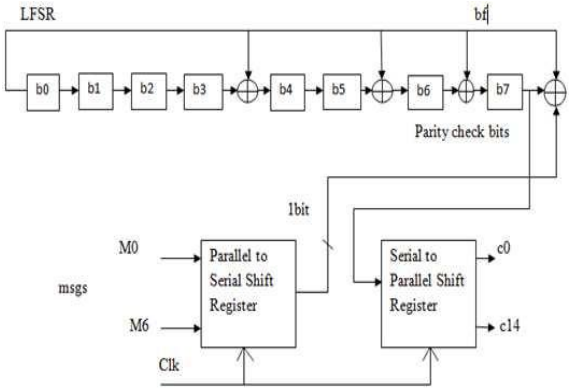

Figure-1: Block diagram of (15,7) BCH Encoder

- The 7 message bits (M0, M1….M6) are applied to the parallel to serial shift register.
- The output of parallel to serial shift register will be sent to (15, 7) BCH Encoder module
- Using these message bits, parity bits are computed and sent to serial to parallel shift register.
- Then parity bits are appended to original message bits to obtain 15 bit encoded data.
- This entire encoding process requires 15 clock cycles.

BCH DECODER:

The decoding algorithms for BCH codes have been developed by Peterson, Goren- stein, Zierler, Chien, Forney, Berlekamp, Massey, Burton and others. A (15, 7) BCH decoder is as shown in fig -2.

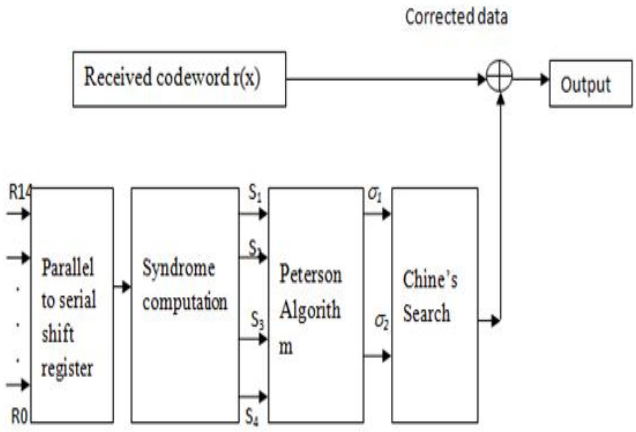

Figure-2: Block diagram for (15, 7) BCH Decoder

- The decoding algorithm for BCH codes consists of three major steps.
- Calculate the syndrome value Si, i=1,2,….,2t from the received word r(x).
- Determine the error location polynomial s*(x)*
- Find the roots of *s(x)* and then correct the errors

The syndrome is the receive sequence multiplied by the transposed parity check matrix H. S (x) =r(x) * HT . The syndrome is a (n-k)-tuple that has a one to one correspondence with the correctable error patterns. The syndrome depends only on the error pattern and is

independent of the transmitted codeword. Most codes do not use all of the redundancy that has been added for error correction. The only two codes known to do this are Hamming (2m- 1, 2m- m - 1) and Golay codes. These codes are called perfect codes.

III RESULTS

Simulation results for multi bit error correction..

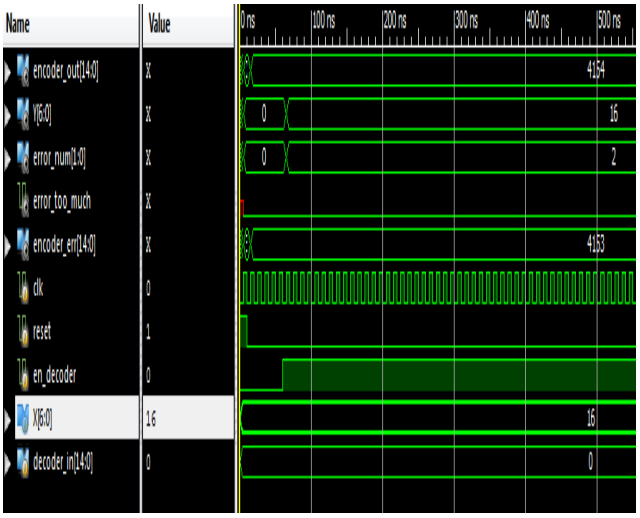

Fig 3: Simulation result.

Table: parameter analysis of the implementation.

S.no	Area (slices & LUTs)	Delay
1	531	4.13ns

IV CONCLUSION

Hamming filtering is based on applying ECC's to the parallel filter outputs to detected and correct error. In which at a single cycle it accepts one bit as an input it can detect two error and clear one bit error through which there will be an increase in the delay ,therefore throughput of the system is reduced drastically. Hence by analyzing these factor ,To enhance the performance of area and delay , BCH code is introduced at a single cycle it can accept n-bit as input and two error can be detected and corrected by using Peterson's algorithm and chine's search algorithm. Experimental results of Hamming filter shows that the performance is satisfactory, hence in the proposed approach of BCH code the result will be enhanced to reduced the area and delay. A (15,7) BCH Encoder and Decoder are more advantageous over than other codes; according to speed requirement.

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BIOGRAPHY

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