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Performance Comparison of Comparators in ADCs using Geometric Programming

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Abstract*: Nowadays, the digitization becomes popular in our society. But all the natural signals are in analog form and need to convert the analog signal into digital signals, analog to digital converters are important .Comparator is the important building block of the data convereter.To optimize the circuit in this work we have introduced the Geometric Programming. Using the Geometric Programming different types of comparator circuits are simulated and output parameters are compared. The resultant values of parameters are tabulated .*

keywords*:Op-Amp based comparator, static comparator ,Matlab ggplab Toolbox*

1.INTRODUCTION

All the signals are analog in nature. In any systems, analog to digital converters and digital to analog converters used widely. Hence the designing the data converters becomes important. As shown in Fig.1,more types of analog to digital converter for different applications. For high speed , low resolution A/D conversions, flash and pipeline ADC's are mostly used. The successive approximation ADC[1] provides moderate conversion speed and moderate resolution. The delta-sigma ADC is used for medium or low speed and high resolution analog to digital conversions. The dual slope ADC is used for the purpose of very high resolution and very low-speed applications. The incremental ADC is same as a delta sigma ADC with periodical reset. The incremental ADC gives the higher resolution and faster in speed than the dual-slope ADC. To optimize the analog and digital converters much work has to be done previously. Automation algorithms can be broadly classified into following to optimize the circuits are:

- Evolutionary algorithms, generic population based meta heuristic optimization algorithms[2] like Genetic algorithms and genetic programming.
- Linear constrained optimization like Integer programming for basic analog cell design[3].
- Stochastic pattern search for designing two stage and cascaded amplifier, which incorporates probabilistic elements[4].

All the methods consumes a lot of time and can also get stuck in local optima because of it uses a simulation tool as a part of the optimum loop.

In this work by using the geometric programming for automating the design of analog to digital converters.

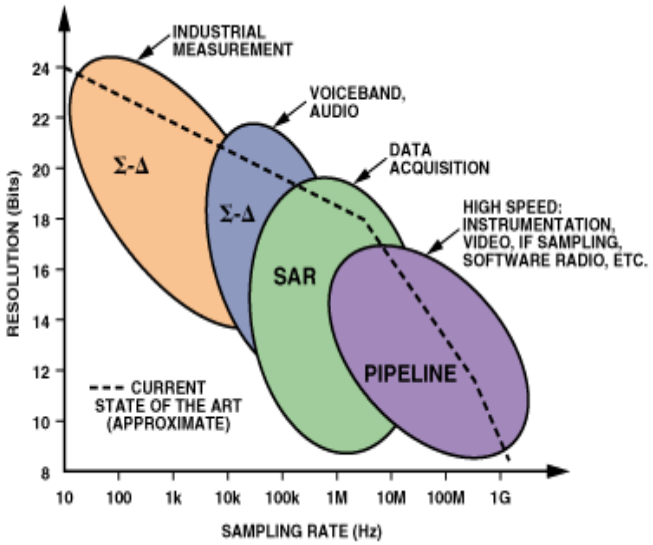

Figure 1.1 ADC architectures for different applications

This work is organized as follows:

- About the geometric programming optimization and its application to circuit sizing is explained in section 2.
- The design procedures of op-amp based comparator is explained in section 3.
- The fourth section describes about design perspective of static comparator.

2. Geometric Programming

Geometric Programming based work has to be starts

in 1980s.In recent days GP has been used for the optimization of mixed signal circuit problems[11-13].

Let x be a vector ($x_1, x_2 \dots . x_m$) of m real, positive variables.

The optimization problem of the form

$$\text{minimize } f_0(x)$$

such that $f_i(x) \leq 1, i = 0,1,2,3 \dots \dots m$

$$g_i(x) = 1, i = 0,1,2,3 \dots . p \quad (2.1)$$

$$x(i) > 0, i = 0,1,2,3 \dots \dots \dots \dots \dots n.$$

Where $f_0(x)$ is the objective function and $f_i(x)\ and\ g_i(x) are$ in equality constraints respectively.

Here, in these constraints $f_0, \dots, f_m$ are posynomial functions and $g_1, \dots g_p$ are monomial functions. Posynomial function has the form

$$f(x_1, \dots, .. x_m) = \sum_{k=1}^{t} c_k\, x_1^{a_{1k}} x_2^{a_{2k}} \dots x_m^{a_{mk}} \quad (2.2)$$

Where $c_j \geq 0$ and a_{ij} are real variables. In the above sum equation, f is called a monomial function. A geometric programming can be converted into the convex optimization problem by changing the variables and takes the logs of the function. The guaranty of a globally optimal solution is provided by the convexity property.

The problem presented in (2.1) is not a convex optimization problem. It can be converted into convex problem by applying 'log' as $y_i = log x_i$ for all $i = 1,2, \dots . , n.$

For any monomials g defined in (2.1)

$$g(x_1, x_2, \dots . , x_n) = g(y_1, y_2, . . , y_n) = c e^{y_1 \alpha_1} e^{y_2 \alpha_2} \dots . e^{y_n \alpha_n} = e^{a^{\sim T} y + b} \quad (2.3)$$

Where $a^{\sim T} = [\alpha_1, \alpha_2, \dots \alpha_n]$ and b , For any posynomial defined in (2.2),

$$f(x_1, x_2 \dots \dots . x_n) = f(y_1, y_2, \dots . . y_n) = \sum_{k=1}^{m} c_k\, e^{y_1 \alpha_{1k} k} e^{y_2 \alpha_{2k}} \dots . . e^{y_n \alpha_{nk}} = \sum_{k=1}^{m} e^{a^{\sim T} y + b_k} \quad (2.4)$$

Where ${\alpha_k}^{\sim T} = [\alpha_{1k}, \alpha_{2k}, \dots \alpha_{nk}]$ and $b_k = log c_k$ for all k=0,1,2,..m.

The Geometric Programming in (2.1) is rewritten as an optimization in the variable $y \ni R^n$ as

$$\text{Minimize } \sum_{k=1}^{m} e^{{a_{ik}}^{\sim T} y + b_{0k}} \text{h}$$

that

Such that

$$\sum_{k=1}^{m} e^{{a_{ik}}^{\sim T} y + b_{ik}} \leq 1; i = 1,2, \dots . . m \quad (2.5)$$

$$e^{{a_{ik}}^{T} y + b_{ik}} = 1; i = 1, \dots \dots p$$

Applying the logarithms to the objective and constraints functions in (2.5),

Minimize

$$f_0(y) = \log\left(\sum_{k=1}^{m} e^{a_{0k}^{T} y + b_{0k}}\right)$$

Such that $f_i(y) = \log\left(\sum_{k=1}^{m} e^{a_{ik}^{T} y + b_{ik}}\right) \leq 1); i = 1, \dots m$

In the above formulation functions f_i are convex functions in their argument y.h_i is an affine function.

Thus, equation (2.6) is a convex optimization problem.

The formulation in (2.6) is equivalent to the standard Geometric Programming in (2.1)

3. comparators

Comparator is the device that compares two analog voltages or currents and switches it output to indicate which is larger[5]. Comparator is a hardware circuit which deals with analogue and as well as mixed mode signals. comparator circuits are optimized for power under constraints on gain, dimension and delay. In this work, designing and comparison of the op-amp based comparator and static comparator be done. Most of the objective functions and constraints are either monomials or posynomials , Geometric Programming is used for the purpose of optimization. The comparison done by using Tanner 45nm technology.

3.1 Op-amp based comparator

This section describes the Geometric Programming model for an Op-Amp based comparator[6] ,the constructions of the objective function, constraints and simulation of optimization results.

The comparator satisfies its requirement that it should be having high voltage if $V_{in}^{+} > V_{in}^{-}$,and a low logic otherwise. The limitation of Op-Amp based comparator is that its input voltage is limited by the common mode input range of the Op Amp, and it results the slow response time. Slow response time may limits the slew rate also.

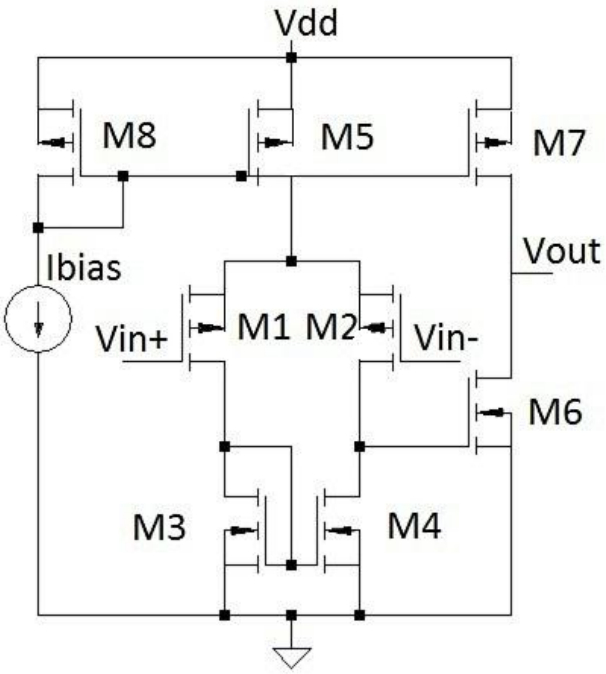

Figure 3.1 An Op-Amp based comparator

To improve the accuracy of Geometric Programming ,the following model should be consider as:

$$I_{Dn} = k_1 W^{a1} L^{b1} V_{ov}^{c1}$$

$$I_{Dp} = k_2 W^{a2} L^{b2} V_{ov}^{c2}$$

$$V_{ovp} = k_4 I_D^{a4} W^{b4} L^{c4}$$

$$V_{ovn} = k_3 I_D^{a3} W^{b3} L^{c3}$$

$$g_{mn} = k_5 I_D^{a5} W^{b5} L^{c5}$$

$$g_{mp} = k_6 I_D^{a6} W^{b6} L^{c6} \qquad (3.1)$$

$$g_{dsn} = k_7 I_D^{a7} L^{C7}$$

$$g_{dsp} = k_8 I_D^{a8} L^{C8}$$

Where $a_1, b_1, c_1, etc.$, are the constants estimated by the Least Square Error(LSE)fitting method.

4.Static Comparator

A static latch based comparator having the advantages compares to the Op-Amp based comparator[7]. A static comparator can be divided into two stages:

- The input stage
- Decision stage

The input stage converts the input voltages to currents, these currents are used to drive decision stage. The decision stage is a cross coupled latch circuit which has two stable states;

the positive feedback of the cross-coupling yields high speed switching.

The problem formulated in the preamplifier and decision stage.

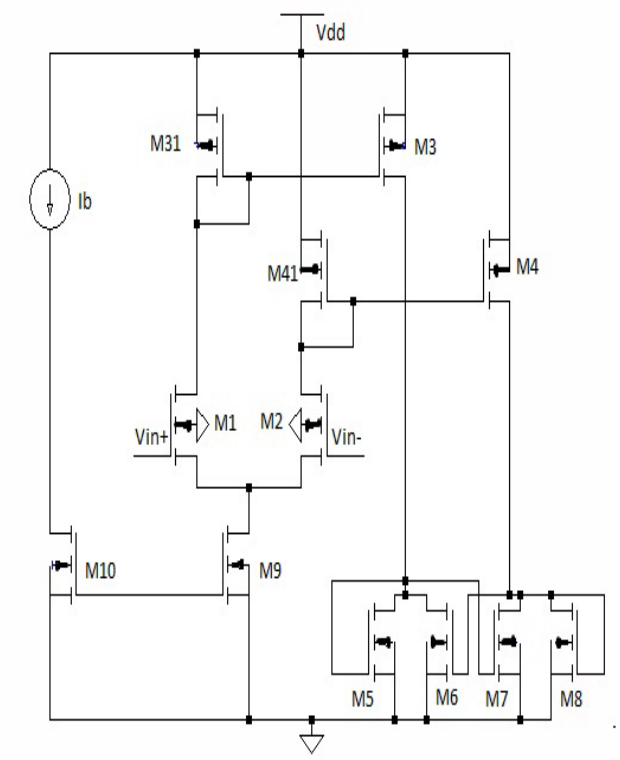

FIGURE 4.1:Schematic diagram of Static Comparator

Preamplifier:

Pre amplifier is a differential amplifier with diode connected loads[9].

Transistors M_1, M_2, M_{31}, M_{41} and M_9 aggregate preamplifier in figure 4.1.

Objective function:

The function to be diminished is power dissipation. The power taken by the preamplifier is given by

$$P = V_d(I_1 + I_2) \quad (4.1)$$

Where I_1 and I_2 are the currents in transistors M_1 and M_2 respectively. P is a posynomial function of the design parameters. Hence the this function considered as objective function to optimize the static comparator circuit.

Constraints:

Dimension, symmetry, biasing, open loop gain and slew rate are considered as the constraints. The constraints defines the design space for the optimum objective function. The mathematical models discussed in this section below.

Dimension constraints:

The following constraints would satisfy the symmetry and matching conditions.

$$W_1 = W_2, W_3 = W_4, L_1 = L_2, L_3 = L_4 \quad (4.2)$$

M_9 and M_{10} are current mirror transistors. Therefore, the lengths of the two transistors are same.

$$L_9 = L_{10} \quad (4.3)$$

To make the transistors M_1, M_2, M_{31} andM_{41} in saturation region, for all possible values of the input common-mode voltage and the output signal swing, bias constraints are applied.

Transistors M_1 and M_2 to be I b saturation region, the condition to be satisfied is

$$k_3 I_1^{a3} W_3^{b3} L_3^{c3} \leq V_{cm,min} - V_{SS} - V_{tp} - V_{tn} \quad (4.4)$$

Gain and Delay constraints:

Open loop gain:

Open loop gain can be calculated as

$$A_v = \frac{g_{m1}}{g_{m3}} \quad (4.5)$$

This equation should be written in a monomial model as

$$\frac{k_5 W_1^{a5} L_1^{b5} I_1^{c5}}{k_6 W_3^{a6} L_3^{b6} I_3^{c6}} \leq A_v \quad (4.6)$$

Delay: Delay can be derived as follows

$$t_{pd} = 0.693 C_L \left(\frac{1}{g_{m3}} \| r_{o3} || r_{o1}\right) \quad (4.7)$$

Where

$$C_L = \left(C_{dp1} + C_{dn1}\right) + \left(C_{gp3} + C_{gn3}\right) + C_W$$

is a posynomial.

Delay expression is a perfect Geometric Programming constraint.

Decision stage:

A pair of PMOS transistors and a cross coupled latch forms a decision stage. Latch speeds up the decision operation using the positive feedback[9].

Objective function:

The objective function is power because of the power is the most important parameter in the Geometric Programming calculation[10]. Power should be calculated as follows:

$$Power = V_{dd}(I_{d3} + I_{d4}) \quad (4.8)$$

Constraints:

Dimension , open loop gain and propagation delay are considered as constraints.

Dimension constraints:

The sizes of the transistors M_{31} $and M_{41}$ of preamplifier. The ratio will be according to the current requirement of decision stage.

$$\frac{W_3}{L_3} = k\frac{W_{31}}{L_{31}}\frac{W_4}{L_4} = k\frac{W_{41}}{L_{41}} \quad (4.9)$$

And $\frac{W_4}{L_4} = k\frac{W_{41}}{L_{41}}$ (4.10)

Where $k = \frac{I_{d31}}{I_{d3}}$

The sizes of latch transistors are given below

$$\frac{W_5}{L_5} = \frac{W_8}{L_8} \quad (4.11)$$

$$\frac{W_6}{L_6} = \frac{W_7}{L_7} \quad (4.12)$$

$$\frac{W_6}{L_6} \leq \frac{W_5}{L_5} \quad (4.13)$$

$$\frac{W_7}{L_7} \leq \frac{W_8}{L_8} \quad (4.14)$$

The constraints which are described in (4.13) and (4.14) are necessary to avoid infinite delay in latch because of large negative resistance.

Gain and Delay constraints:

Open loop gain:

The open loop gain can be expressed as

$$A_v = \frac{g_{m3}}{g_{m5} - g_{m6}} \quad (4.15)$$

$$A_{v1} \leq \frac{g_{m5} + g_{m6}}{g_{m5} - g_{m6}} \quad (4.16)$$

And $A_{v2} \leq \frac{g_{m3}}{g_{m5} + g_{m6}}$ (4.17)

But these equations are not a perfect geometric programming constraints.

$$A_{v2}(g_{m5} + g_{m6}) \leq g_{m3} \quad (4.18)$$

5. Simulation Results:

For Op-Amp comparator:

Objective Function						
Power(μW)	7	9	7	15	146	243
Constraints						
Gain(dB)	70	70	84	75	60	54
Delay(ns)	50	25	50	15	10	5
Design Variables						

$W_1=W_2$(µm)	1.6	1.89	1.62	2.07	2.97	2.70
$W_3=W_4$(µm)	0.9	1.26	0.99	1.46	4.41	3.96
W_5(µm)	1.1	0.99	1.17	0.99	0.99	0.99
W_6(µm)	0.9	0.99	0.99	0.99	0.99	0.99
W_7(µm)	0.9	0.99	0.99	0.99	1.35	0.99
W_8(µm)	2.2	1.08	2.25	0.99	0.99	0.99
$L_1=L_2$(µm)	3.1	2.79	3.24	2.79	3.42	2.70
$L_3=L_4$(µm)	5.0	4.05	5.04	3.60	3.87	3.60
L_5(µm)	0.9	0.63	0.99	0.63	0.45	0.45
L_6(µm)	2.8	1.26	2.79	0.81	0.27	0.18
L_7(µm)	0.9	0.63	0.99	0.63	0.45	0.45
L_8(µm)	0.9	0.63	0.99	0.63	0.45	0.45
Vodn(V)	0.1	0.10	0.10	0.11	0.18	0.23
Vodp(V)	0.1	0.14	0.11	0.15	0.48	0.69
Ibias(µA)	1.0	1.00	1.00	1.33	13.35	26.70
Matlab Results						
Gain(dB)	86	81	85	77	62	56
Delay(ns)	50	25	50	15	10	5

Table 5.1:Open loop comparator simulation results

For Static latched comparator:

Objective Function						
Power(µW)	5	7	5	18	35	35
Constraints						
Gain(dB)	70	70	84	60	54	60
Delay(ns)	50	25	50	10	5	5
Design Variables						
$W_1=W_2$(µm)	1.2	1.2	1.2	1.2	1.2	1.2
$W_{31}=W_{41}$(µm	1.7	1.3	1.7	0.9	0.99	0.99
$W_3=W_4$(µm)	0.9	0.99	0.99	0.99	0.99	0.99
$W_5=W_8$(µm)	0.9	0.99	0.99	0.99	0.99	0.99
$W_6=W_7$(µm)	0.9	0.99	0.99	0.99	0.99	0.99
W_9(µm)	0.9	0.99	0.99	0.99	0.99	0.99
W_{10}(µm)	0.9	0.99	0.99	0.99	0.99	0.99
$L_1=L_2$(µm)	0.9	0.9	0.99	0.99	0.99	0.99
$L_{31}=L_{41}$(µm)	1.4	1.71	1.44	1.80	2.43	2.43
$L_3=L_4$(µm)	4.2	3.78	4.23	2.70	1.80	2.43
$L_5=L_8$(µm)	3.5	3.60	3.51	0.81	0.54	0.54
$L_6=L_7$(µm)	3.7	3.69	3.78	0.90	0.63	0.72
L_9(µm)	0.5	0.54	0.54	0.54	0.54	0.54
L_{10}(µm)	0.5	0.54	0.54	0.54	0.54	0.54
Vodn(V)	0.1	0.10	0.10	0.12	0.17	0.17
Vodp(V)	0.1	0.13	0.12	0.23	0.37	0.37
Ibias(µA)	1.0	1.00	2.12	3.24	3.24	3.24
Matlab Results						
Gain(dB)	80	81	85	64	58	63
Delay(ns)	50	25	50	15	5	5

Table 5.2: Static comparator simulation results

6.Conclusion:

We have described a Geometric Programming to

optimize the circuits. In this work two types of comparators are designed and simulated. Geometric Programming had to be used for optimizing the comparator circuits. The simulation has to be done by using the Matlab ggplab Tool box and the results are to be tabulated. The comparison of Op-Amp based comparator and Static comparator should be done in this work.

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